REMARKS

Claims 1 through 3 are currently pending in the application.

This amendment is in response to the Office Action of August 9, 2006.

35 U.S.C. § 112 Claim Rejection

Claim 1 is rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention.

Applicant has amended the claimed invention as suggested by the Examiner for the presently claimed invention to particularly point out and distinctly claim the subject matter of the invention to comply with the provisions of 35 U.S.C. § 112. Therefore, presently amended claim 1 is allowable under the provisions of 35 U.S.C. § 112.

35 U.S.C. § 103(a) Obviousness Rejections

Obviousness Rejection Based on Yabe (U.S. Patent No. 5,726,074)

Claims 1 through 3 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Yabe (U.S. Patent No. 5,726,074) in view of Di Zenzo et al. (U.S. Patent No. 6,130,442). Applicant respectfully traverses this rejection, as hereinafter set forth.

Applicant asserts that to establish a *prima facie* case of obviousness under 35 U.S.C. § 103, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Third, the cited prior art reference must teach or suggest all of the claim limitations. Furthermore, the suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on Applicant's disclosure.

Turing to the cited prior art, the Yabe reference teaches or suggests the use of a bar code applied to a wafer to store information regarding the plurality of semiconductor integrated circuits formed on the wafer.

The DiZenzo et al. reference teaches or suggests recording information about failure rates in testing within the semiconductor chip regarding the specifications as established in connection with the various device categories.

Applicant asserts that any combination of the Yabe reference and the DiZenzo et al. reference does not and cannot establish a prima facie case of obviousness under 35 U.S.C. § 103 regarding the claimed inventions of presently amended independent claims 1, 2, and 3 because any combination of such cited prior art fails to teach or suggest all the claim limitations of the claimed inventions. Applicant asserts that the Yabe reference does not identically describe the element of the claimed inventions of presently amended independent claims 1, 2, and 3 calling for "storing an enhanced reliability testing flag in the integrated circuit device associated with a unique identification code of each integrated circuit device of the plurality of integrated circuit devices for indicating whether each integrated circuit device requires enhanced reliability testing" and "storing a reliability testing flag in the integrated circuit device associated with a unique identification code of each integrated circuit device of the plurality of integrated circuit devices for indicating whether each integrated circuit device requires further reliability testing". In contrast to the claimed inventions of presently amended independent claims 1, 2, and 3 of the present application, the Yabe reference stores information on the wafer using a bar code regarding the speed of the semiconductor integrated circuit while the DiZenzo et al. reference stores information regarding the testing of the integrated circuit chip, not the requirement of needing enhanced reliability testing. Such is not the claimed inventions of presently amended independent claims 1, 2, and 3. Therefore, such claims are allowable.

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Applicant submits that claims 1 through 3 are clearly allowable over the cited prior art.

Applicant requests the allowance of claims 1 through 3 and the case passed for issue.

Respectfully submitted,

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